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13. ABSTRACT (Maximum 200 words)
The objective of our research is to demonstrate "smart" spatial light modulators (S-SLM) where electronic logic circuits are combined with light modulators and detectors. Our previous studies, while providing valuable insights, indicated that shortcomings of certain approaches limit their applicability to combine Si-based driver and logic circuits with PLZT modulators. For example, PLZT films deposited onto windows of SOS were too thin to provide useful light modulations, while the trade-off between improvement in recrystallized Si quality and PLZT substrate damage limited laser recrystallization approach. Lastly, voltage compatibility problem exists that imposes difficulties in the integration of the modulator driver circuit (requiring 30-50V) in the Si-waver containing logic circuits (operating at 5V). In order to resolve these limitations we explored (i) two methods of implementing thin films of Si-band driver circuits directly onto PLZT substrate and (ii) flip-chip bonding of Si wafer containing detector and logic circuits onto the silicon bonded directly to bulk PLZT substrate for fabrication of S-SLM. The cross section of a unit cell of fully integrated S-SLM illustrated in Figure 1.

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1. Introduction

The objective of our research is to demonstrate "smart" spatial light modulators (S-SLM) where electronic logic circuits are combined with light modulators and detectors. Our previous studies, while providing valuable insights, indicated that shortcomings of certain approaches limit their applicability to combine Si-based driver and logic circuits with PLZT modulators. For example, PLZT films deposited onto windows of SOS were too thin to provide useful light modulation, while the trade-off between improvement in recrystallized Si quality and PLZT substrate damage limited laser recrystallization approach. Lastly, voltage compatibility problem exists that imposes difficulties in the integration of the modulator driver circuit (requiring 30 - 50V) in the Si-wafer containing logic circuits (operating at 5V). In order to resolve these limitations we explored (i) two methods of implementing thin films of Si-based driver circuits directly onto PLZT substrate and (ii) flip-chip bonding of Si wafer containing detector and logic circuits onto the silicon bonded directly to bulk PLZT substrate for fabrication of S-SLM. The cross section of a unit cell of fully integrated S-SLM is illustrated in Figure 1.

2. Summary of the Results

During the first 5 months period of our research, we were successful in implementing functional Si-transistors onto PLZT substrates via *1*) bonding thin (2-4μm) Si wafer to PLZT and processing and 2) directly bonding prefabricated NMOS transistor array to PLZT substrate. The resulting modulators were characterized for the development of next generation S-SLM. We have also modeled the operation of a light modulator based on multilayer thin films of ferroelectric materials such as PLZT, PBN, SBN to investigate the optimum material and device structure both from application and fabrication aspects. This progress report summarizes the results of first phase of the research.

2.1 Bonding of Silicon films on PLZT

We investigated two direct bonding (DB) techniques for combining thin silicon films with bulk PLZT: *1*) bonding of commercially available 2-4 μm thick silicon films onto PLZT, followed by the fabrication of MOS devices, 2) fabrication of MOS devices in SOI Si wafers, followed by the lifting of thin Si film containing devices and bonding to bulk PLZT. Commercially available films are thicker and have excellent lifetime providing a suitable Si layer for future CMOS or bipolar device implementations and detector fabrication for optically addressed SLMs. However, temperatures of the device fabrication steps need to be lowered to avoid damage to the underlying PLZT substrate when approach (1) is applied. The transfer of the prefabricated devices onto PLZT eliminates potential

PLZT damages resulting from high temperature device processing steps, since all the device fabrication takes place before joining Si with PLZT. However, the transfer and bonding techniques are more critical to insure good device performance after bonding.

2.1.1 Bonding Si Film onto PLZT for MOS Circuit Fabrication

2.1.1.1 Fabrication of MOS Circuit on Bonded Si Film

In this approach, a high quality commercially available thin (2-4μm) Si film is bonded onto a transparent PLZT substrate and processed. A low temperature MOS processing steps are then applied to avoid thermal damage to the PLZT substrate.

A test mask was designed with various MOS Transistors gate widths and lengths. The first goal was to investigate the fabrication steps and resulting device characteristics in bonded Si films on PLZT as well as the characterization of the modulator connected to the Si devices. For this purpose, as an initial step, two inch diameter, 4μm thick, p-type, <100> orientation Si films from Virginia Semiconductor Inc. were bonded to <1102> oriented sapphire as well as to PLZT substrates and sequenced through low temperature metal gate NMOS transistor fabrication process.[1] Standard Si wafer cleaning methods were employed, but special attention was paid to avoid wafer damage by excessive agitation. Sapphire substrate was pretreated in 10% HF solution. PLZT substrate was coated by PECVD silicon dioxide and sputtered aluminum oxide to promote adhesion. The cleaned Si film was placed over the substrates in de-ionized water. The resulting structure was then processed through low temperature (<850 °C) NMOS fabrication steps illustrated in Figure 2. A portion of the PECVD deposited SiO_2 film, which serves as ion implantation mask, was left to clamp the isolated Si islands to substrate in addition to the Van der Waals bonding.

2.1.1.2 Performance of MOS Circuit Fabricated on Bonded Si Film

Metal gate NMOS structures of various gate widths and lengths were fabricated onto the bonded Si films. Photo-micrographs of a finished device is shown in Figure 3. These devices exhibited electrical performances that were comparable to that of similar devices fabricated on bulk Si.[2] The threshold voltages of these devices were distributed between 1.0 to 1.2V for all gate lengths (5, 10 and 15 μm). The source-drain breakdown occurred at about 25V, exhibiting a distinct avalanche behavior. The leakage current was about 20pA for 10μm gate widths for most of the transistors. A typical I-V curve for a 10μm length by 20μm width gate size transistor is shown in Figure 4. The electron mobility, calculated from the I-V curve shown, is 440 $cm^2/V\text{-}s$. This value is lower but comparable

to that of devices fabricated on bulk Si. The transconductance of the transistors were approximately 100 μS at V_{DS} = 10V for V_G = 0 - 5V.

2.1.2 Transfer and Bonding of Prefabricated MOS Circuit onto PLZT

2.1.2.1 Fabrication and Transfer/Bonding of MOS Circuit

In exploring an alternative approach to combine Si circuits with PLZT, we succeeded in isolating, transferring, and bonding thin (1.6 - 2.0 μm) Si film with prefabricated devices onto PLZT substrate. Although such technology for transferring GaAs-based circuits has been investigated by various groups for some time, those studies provide only a guideline for Si-based system.[2]

For this purpose, commercially available SOI wafers from KOPIN Corp. with 0.6 - 1.0 μm thick bulk-quality Si film on top of 1.0 μm thick SiO_2 layer on a host Si substrate were used. A test structure consisting of NMOS transistors of various gate widths and lengths were fabricated on these wafers by applying a conventional NMOS process. The host Si substrate was removed by mechanical grinding to ~100 μm thickness followed by chemical (KOH) etching from the back side. Here, the SiO_2 layer provides a self-termination point for the chemical etching step. The resulting film consisting of isolated Si islands on SiO_2 layer was then transferred onto PLZT substrate and bonded using an adhesion layer of polyimide. This process is illustrated in Figure 5. This approach allows standard commercial Si processing steps to be applied during device fabrication. The advantage of imposing no limitation on the NMOS processing parameters should be self-evident.

2.1.2.2 Performance of Transfer/Bonded MOS Circuit

Photomicrographs of MOS devices before and after etching (Figures 6(a) and & 6(b), respectively) show no discernible degradation in surface quality due to the etch/transfer/bonding steps. Using this method, we were able to transfer approximately 10 X 10 mm circuit area onto a new substrate. We also cooperated with KOPIN Corp. to demonstrate the scalability of the transfer and bonding of areas as large as 50 mm x 50 mm. KOPIN uses a thick (> 10 μm) epoxy as a glue for bonding. Our polyimide alternative will result in a thinner interface layer (< 1.5 μm) which is crucial in establishing good electrical contact between the output transistor and the modulator.

The transferred devices exhibit only a slight change in electrical performance. The I-V curves of NMOS transistors of same gate size (W=10μm and L=20μm) before and after the transfer process are compared in Figure 7. Threshold voltage of the control sample (remaining on the SOI wafer) was in the range .8 to .9 V. V_{BR} of both control and

transferred samples were about 15V. About 0.25 V shift in threshold voltage along with a slight increase in trasconductance from 39 μS to 41 μS is observed at V_{DS} = 10 V and V_G = 0 - 5V after the transfer. The change in interface charge at the bonding interface is most likely the cause of the observed variations. Specific mechanisms responsible for the observed changes are under investigation.

Both the control and transferred transistor samples were connected in NMOS inverter configuration with external load and transistor load (enhancement load) and characterized. For low supply voltages (e.g.V_{DD} = 5V), gate sizes for optimal W/L gate size ratio between the load and inverter transistor were available on the test structure. Figure 8a shows the inverter configuration and the output voltage curve for a square wave input. The curve shows a rise time of 20μsec. For supply voltages larger than 10 V, optimal gate size combinations were not available for transistor load inverter connection. Thus, the transistors were characterized with external load for subsequent measurements where V_{DD} ≥ 10V. The measurements results given in Figure 8b indicate that maximum output contrast is ~20 V for V_{DD} = 40 V. Further increase in V_{DD} only shifted the same contrast curve up slightly without increasing the contrast. This is not surprising since V_{BR} of these devices are ~20 V. The single transistor contrast may be improved by controlling the process parameters to obtain a higher V_{BR}. This can be obtained readily since in the previous section, it was shown that similar transistors produced under less ideal process parameters resulted in V_{BR} = 25 V.

In order to obtain modulator contrast better than 100 with bulk PLZT, approximately 50 V must be applied to 10 μm spaced electrodes. In order to meet such requirement with transistor load, in addition to improving the V_{BR} and optimizing the gate sizes, an alternative configuration consisting of multiple transistors connected in series to distribute the voltage difference need to be considered.[3] All of these issues will be studied and resolved in the coming year for the design of functional S-SLM.

2.2 Flip-Chip Bonding

Flip-chip bonding with solder provides self-alignment which is critical for the assembly of optoelectronic devices such as S-SLM (Figure 1). Progresses in design and fabrication of solder-joint based flip-chip joint for S-SLM are discussed below.

As a first step, the size and the number of solder joints needed to support the PLZT modulator on silicon chip were determined. This is done by optimizing the pad size, pad geometry, and solder volume as a function of the total weight of PLZT acting on the solder joints. Figure 9 shows the profile of the solder joint with 40 μm square pads used for the

assembly. Figure 10 shows load carrying capability of one solder joint in an array of 22 pads supporting the weight of a 350 μm thick PLZT substrate of 2.5 x 2.5 mm area.

Once, the pad size, geometry, and solder volume are finalized, the next step is to fabricate these solder pads on the silicon chip and PLZT sides. The function of the solder pad is to (1) provide solder wetting surface, (2) provide barrier interface between solder material and Al pads on Si chip and PLZT substrate, (3) allow for maximum possible solder reflow time, and (4) allow for multiple reflow. The solder material selected is 63Sn/37Pb for its low melting temperature and ease of deposition through electroplating process.

During in-house fabrication of PLZT modulators, solder can be deposited on PLZT by electroplating process which is best suited for such bulk production. The solder pad composition of Cr/Cr-Cu/Cu was selected for the PLZT since this composition is most suited for post processing of PLZT with electroplated solder joints.

For Si chip, the problem encountered is different. The chip is obtained in diced form from the supplier. This precludes conventional e-beam deposition and subsequent photolithography of the solder pads . This constraint can be circumvented by depositing the solder pad material through electroless-plating process; this process is most suitable for metal deposition on diced components. For electroless-plating of solder pad on Si chip, Ni/Au composition was selected.

Currently we are optimizing the process sequences associated with solder deposition through electroplating and electroless plating of Si chip. Figure 11 illustrates the process sequences for the flip-chip bonding in S-SLM fabrication.

3. Future Work

3.1 8x8 S-SLM Fabrication

Currently, steps are being carried out to design and fabricate an 8x8 S-SLM utilizing the technologies mentioned in the previous section. For this purpose we plan to characterize a modulator cell driven by these transistors. The 8x8 S-SLM will be designed to accommodate both electrical and optical addressing. However, several manufacturing issues must be studied and resolved in order to make these technologies useful for the intended purpose. Physics of bonding two material systems with bonding layer need to be understood for reliability and scalability that will be inevitably required by array fabrication. Also, the specific mechanism responsible for the slight change in device performance need to be identified. Accomplishments to date confirm the feasibility of S-SLM fabrication.

An S-SLM cell must include PLZT modulator driver circuit and some on-board logic capability. Since about 50V need to be applied to a typical modulator window, the

driver design must consider joining two or more transistors in series to avoid breakdown. This requires additional study of transistor fabrication processes and performance for consistency. To have on-board logic capability, XOR and memory circuits need to be implemented into the device film. In addition, we need to carefully design the circuit layout to maximize modulator control and logic capacity within the geometrical constraints of the modulator unit cell. Inevitably, the need to flip-chip bond a detector, detector circuit, and logic circuit array to the modulator array will arise. Hence, features necessary for flip-chip bonding must also be designed into the layout of the unit cell.

The modulator array may be designed to operate in either transmission or reflection mode. If logic circuitry with a detector array is to be flip-chip bonded to the modulator array, then the modulators must operate in reflection mode. This mode of operation may be optimized through the implementation of dielectric stack mirror instead of Al mirror. A possible layout of modulator flip-chip bonded to detector array is illustrated in Figure 1.

After an 8 x 8 array is fabricated and characterized, a scalability study will be conducted, based on its performance characteristics. Possible modifications to improve the device properties such as speed, dynamic range, and uniformity.

3.1.1 8x8 Electrically Addressed S-SLM

To fabricate an 8x8 Si/PLZT electrically addressed SLMs (ESLM), three issues must be resolved in the coming months. These are :

1) an increased V_{BR} (to 35 - 50 V) and reduced leakage current: Adjustment of the resistivity of substrate, simulation of the concentration profile of ion implantation after gate oxidation, and anneal are being considered to produce MOS devices with high V_{BR} and low leakage current. An alternative using two transistors in series with 20-25V breakdown voltage each will be explored to satisfy additional voltage requirement. The issue of final drive speed above MHz range will be taken into account during these modifications.

2) Improved connection between transistors and modulators: DB approach 1 results in a 4 - 5 μm of height difference between transistors and modulators that need to be connected electrically. For DB approach 2, uv sensitive polyimide will be considered as a thin bonding layer (<2 μm thick) to resolve the thickness problem (~12 μm) imposed by the epoxy. For both DB approaches, an accurate control of the height profile and improved step coverage during metallization will be added to allow reliable electrical connection between the transistors and modulators.

3) Special switch/driver design: A SRAM and/or a DRAM like addressing mechanism will be used to select the required pixel(s). However, due to capacitive loading of the modulator and high drive voltage needed to obtain high contrast ratio, the switching cell design needs to be modified. During this modification, the characteristics of the transistors in thin film Si will be also taken into consideration. The block diagram of the 8x8 electrically addressed SLM is shown in Figure 12a. The pass transistor will be used to connect the data line to the requested pixel. The pixel selection will be done by applying voltage to the gate of the pass transistor. When the pass transistor is on, the data will be transferred to the built-in driver that activates the corresponding pixel. Gray scale can be achieved by designing an analog driver and using either an analog or multilevel data input. The 8x8 array will have 8 input pins for row selection and 8 input pins for data (column) and necessary pins for power, ground, etc. Although the pin count can be accommodated by existing packages at moderate array sizes, a demultiplexing circuit need to be added to larger arrays in order to keep the pin count low (Figure 12b). The demultiplexing circuit will get the data and address information in a serial format through a limited number of external input pins and forward them to many internal rows and columns. The multiplexing/ demultiplexing operation may limit the highest frequency of operation for large arrays.

3.1.2 8x8 Optically Addressed S-SLM

As mentioned earlier, 8x8 S-SLM will be designed to accommodate optical addressing, as well as electrical addressing. The optical addressing can be achieved through the detector circuit on the flip-chip bonded wafer. In this scheme, a packaged free-space interconnection would relay the addressing signal to the detector array. The free-space interconnection eliminates the multiplexing and demultiplexing required by the electrically-addressed SLMs since each pixel is addressed directly; this would result in substantially higher frequency of operation for large arrays. The addressing signal will then be processed by the supporting circuit and connected to the gate of the pass transistor of the modulator driver circuit. The remaining operation of optically-addressed S-SLM will depend on the performance of the devices within each cell. Thus, issues discussed in the previous section will also be relevant for the fabrication of optimally performing optically-addressed S-SLM.

3.1.3 Application of 8x8 S-SLM to Page Oriented Holographic Neural Network System

An ongoing research project at UCSD studies large scale optoelectronic general purpose neural network modules. The system curently under design is based on an optical holographic memory that stores binary bit planes of synaptic weights which allow fully parallel reconstruction and partially optical summation at the output neural plane. PLZT based S-SLMs have been selected to achieve optically the multiplication of each page of weights by the corresponding input, conferring to the system a higher parallel throughput than what could be achieved with other SLM technologies. In addition, PLZT based S-SLMs preserve the phase information of the modulated beams. This is required for the mentioned holographic neural network architecture, especially during the learning mode (when an S-SLM is used to record each page of weights into the holographic memory, including the phase corresponding to each SLM pixel), to insure proper reconstruction during relaxation. The size of the modulators on 8x8 S-SLM will be made so that the use of diffractive lenslet arrays can be readily accommodated.

3.2 Ferroelectric Multilayer Thin Film S-SLM

In addition to the reported progress in Si/PLZT DB technology, we are also exploring the possibility of utilizing ferroelectric multilayer thin film as the modulating media, replacing bulk PLZT, for the next generation S-SLM. The multilayer structure will consist of electro-optically active PLZT (quadratic) as the high index material and SBN or PBN (both linear) as the low index material. The multilayer can be designed to operate as a voltage-tunable high reflector (HR) or a tunable asymmetric Fabry-Perot (AFP) filter with a PLZT spacer layer. Compared to the MQW-based multilayer modulators, PLZT-based multilayer modulator structures will have less absorption, which results in higher throughput and less heat conduction problems, although their speed is not as attractive as that of MQW-based structures. Previous studies performed at UCSD have indicated that PLZT films with quadratic electro-optic coefficient of 0.6×10^{-16} m^2/V^2 can be sputtered onto PLZT or sapphire substrates.[3] Technologies for obtaining thick ferroelectric films of PLZT, SBN, and PBN are currently being developed at Rockwell International based on Sol-Gel approach and at Advanced Technology Materials Inc. based on MOCVD approach. Multilayers can be deposited onto foundry-processed Si substrate containing logic and detector circuits.

The operation of ferroelectric multilayer modulator is based on applied field-induced change in refractive indices of constituent layers. By applying field to the structure, refractive indices (n_i) of constituent layers can be changed, effectively changing the optical thicknesses of each layer. Changes in refractive indices will follow,

$$n(V) = n_o - \frac{1}{2} n_o^3 \gamma_i \frac{V^2}{D^2} \quad \text{(for quadratic material)} \qquad (1)$$

$$\text{and} \quad n(V) = n_o - \frac{1}{2} n_o^3 \gamma_i \frac{V}{D} \quad \text{(for linear material)} , \qquad (2)$$

where n_o = refractive index at V = 0, γ_i = electro-optic coefficient, V = applied voltage, and D = electrode spacing. The index modulation will shift the frequency response of the multilayer stack (see Figure 14 for example). Thus, for certain wavelength, the multilayer stack will cause virtually zero reflection at V = 0 and high reflection (R >95%) at some V > 0.

Although the initial calculations omitted some critical effects such as slight absorption, dispersion and interface scattering, the simulation results are promising. Further numerical evaluations that account for these effects and thickness variation of individual layers are planned. As experimental data on the physical properties of deposited films become available, further design optimization will be required.

3.2.1 Multilayer High Reflector

Multilayer HR would consist of alternating layers of ferroelectric layers such as PLZT (n = 2.55) and PBN (n = 2.32) designed for wavelength slightly greater than the wavelength of operation. The application of field shifts the pass-band of the stack toward the shorter wavelength as the optical path lengths of individual film layers decrease according Eqs. (1) and (2). Figure 13 illustrates the structure of the multilayer HR.

The effects of field (V/D) application on reflection spectrum of a 25-period multilayer is calculated in Figure 14. A $\lambda/4$ thick SiO_2 (n ~1.45) matching layer is placed on top of the stack to suppress the reflectance null (at V = 0) from 0.046 to 0.00016. Radiant reflectance for operation at λ_o = 514.5nm of the stack varies from 0.00016 to 0.8967 for applied voltage variation from 0 to 30V; this corresponds to contrast >5000. The contrast suffers -3dB reduction when wavelength deviates ± 0.6Å from the center wavelength λ_o; this occurs consequently as the null at V = 0 increases to ~.00032. The structure tolerates ± 2.2° incident angle variation at λ_o before the contrast suffers -3dB reduction. The reflectance as a function of applied voltage at λ_o = 514.5 nm for a typical HR stack is calculated in Figure 17. The figure illustrates that a smooth transition from low reflectance (~0.00) to high reflectance (>0.90) is readily obtainable for voltage swing of ~40 V. High-pass multilayer filter design is being evaluated as a possible solution to increase the wavelength tolerance.

3.2.2 Multilayer Fabry-Perot Cavity

Multilayer AFP modulator may also be controlled in a manner similar to that of HR stack as discussed in previous section. A typical AFP structure is illustrated in Figure 15. With AFP stacks, thickness of the spacer layer becomes an additional parameter to control the characteristics of the multilayer stack. The null value of AFP stack may also be suppressed by adding an additional top layer to enhanced the matching of reflectivities on opposite sides of the spacer layer.

The effects of field application on reflection spectrum of AFP stack is calculated in Figure 16. Total thickness of the stack is about 3.6 μm. A $\lambda/4$ thick AlF_3 (n~1.38) matching layer is placed on top of the stack. Addition of this layer suppresses the reflectance null from 0.00125 to 0.00043. Radiant reflectance for $\lambda = 514.5$ of the stack varies from 0.00043 to 0.8363 for applied voltage variation from 0 to 30V; this corresponds to contrast of ~2000. Additional calculations indicate that such structure can tolerate wavelength variation of ± 5Å before suffering -3dB decrease in contrast; this occurs consequently as the null (at V = 0) increases to ~.00089. The AFP modulator design tolerates ± 1.55° incident angle variation before contrast suffers -3dB reduction. A comparison of Figures 11 and 13 shows that apparent increase in wavelength tolerance for AFP is due to flatter wavelength response near the operation wavelength. Thus, the initial calculations indicate that AFP stack may offer better wavelength tolerance than the HR stack at the cost of increased overall thickness. The reflectance as a function of applied voltage at $\lambda_o = 514.5$ for a typical AFP stack is calculated in Figure 17. The figure illustrates that a smooth transition from low reflectance (~0.00) to high reflectance (>0.90) is readily obtainable for voltage swing of ~40 V.

4. Conclusions

We have demonstrated for the first time the bonding of thin si films to ferroelectric ceramics such as PLZT and characterized the Si on PLZT device operation. Thin silicon layers will include the high voltage drivers for modulators. When combined with silicon wafers containing logic circuits and detectors by using flip-chip bondind S-SLMs of any complexity can be obtained. We have developed process steps for flip-chip bonding as well. We have also modeled the operation of light modulators based on multilayer thin films. Our future goal is to realize simple 8x8 S-SLMs and necessary design effort is underway.

With these advances, large scale S-SLMs can be realized. These S-SLMs will be able to satisfy the system requirements imposed by high performance digital opto-electronic computing.

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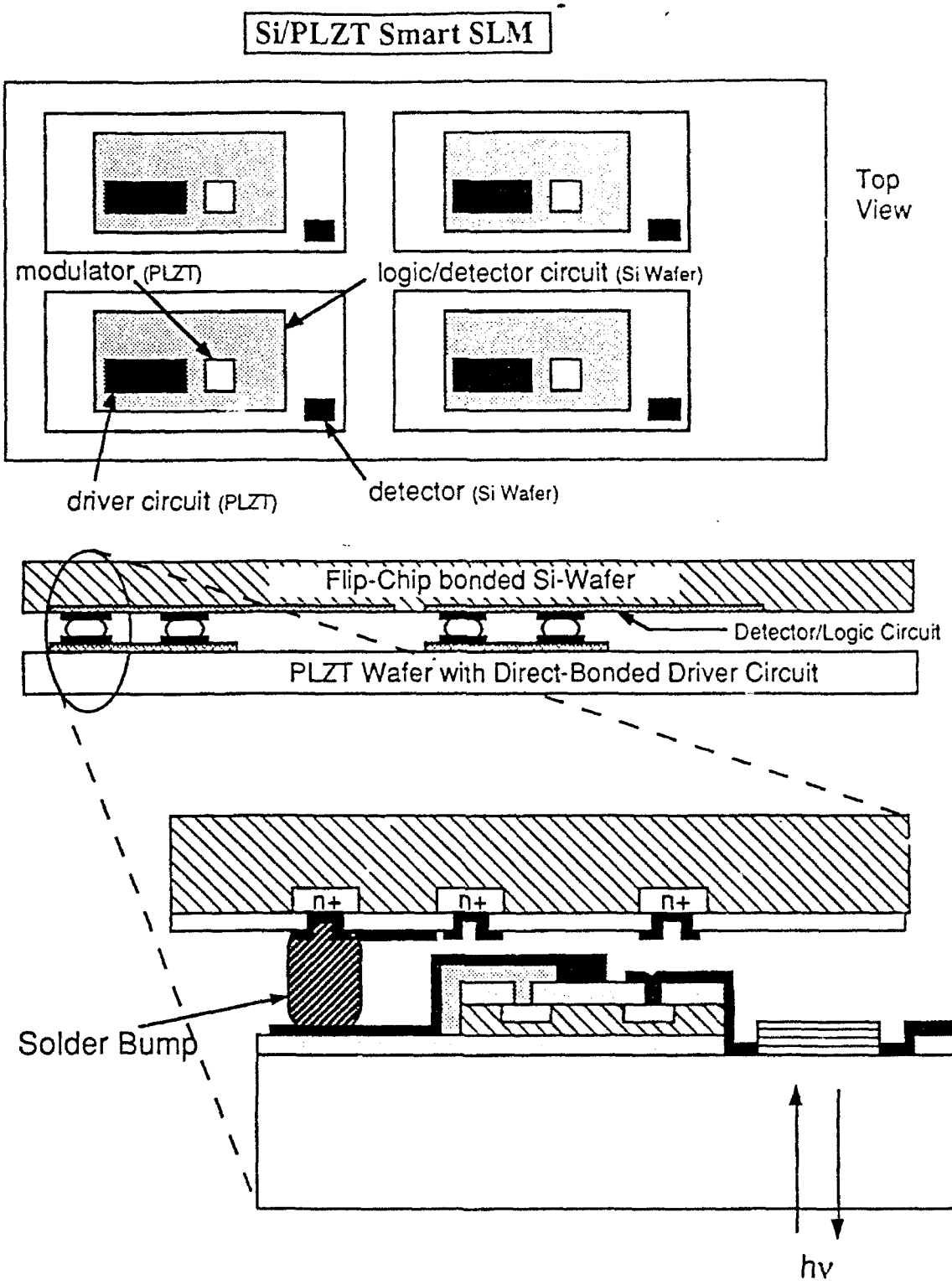


Figure 1. Cross section of one Si/PLZT S-SLM unit cell integrated by using combination of thin Si film bonding to PLZT and flip-chip bonding.

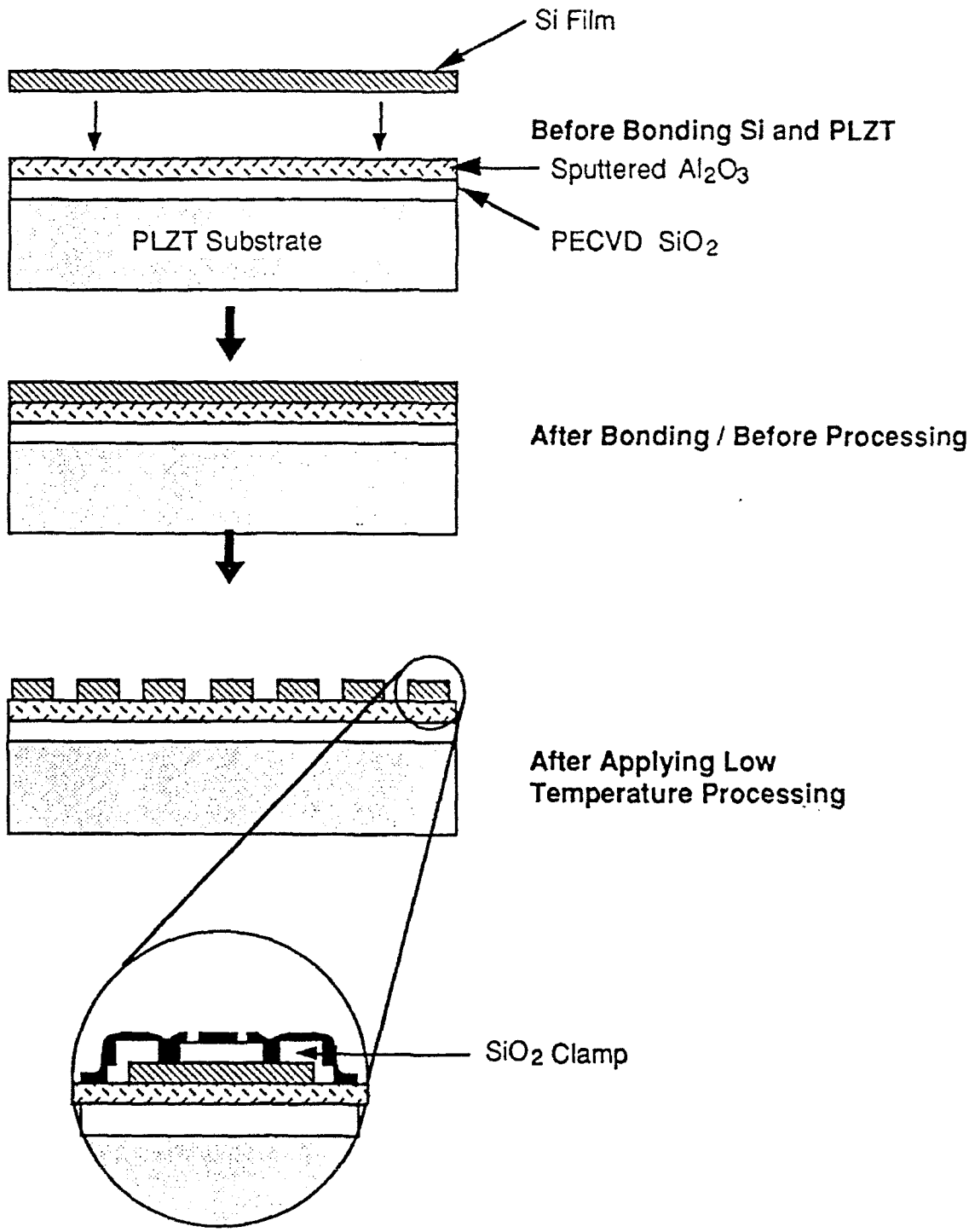


Figure 2. Schematic illustration of processing steps involved in fabricating transistor structures on thin Si wafers bonded onto sapphire/PLZT substrates. Low temperature processing consists of ~850 °C (compared to typical 1050 °C) gate oxidation step.

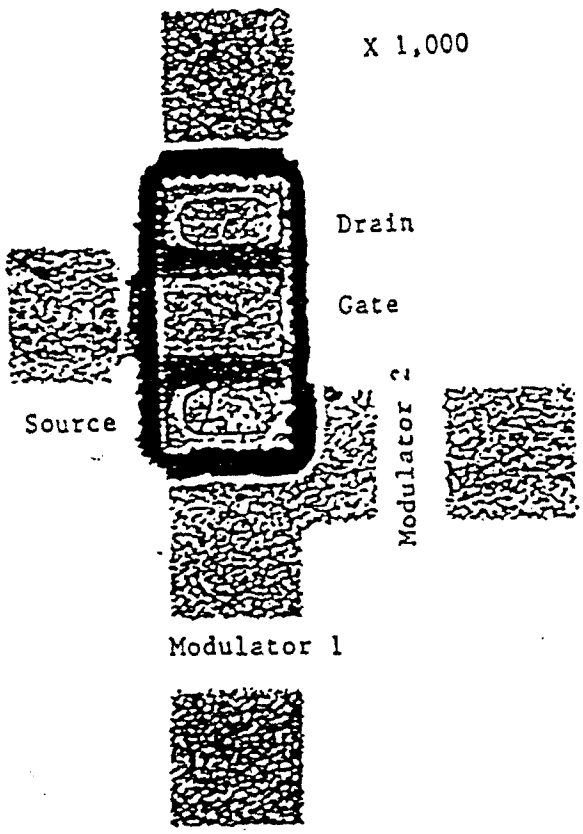


Figure 3. Photomicrograph of NMOS transistor fabricated on Si film bonded onto sapphire substrate.

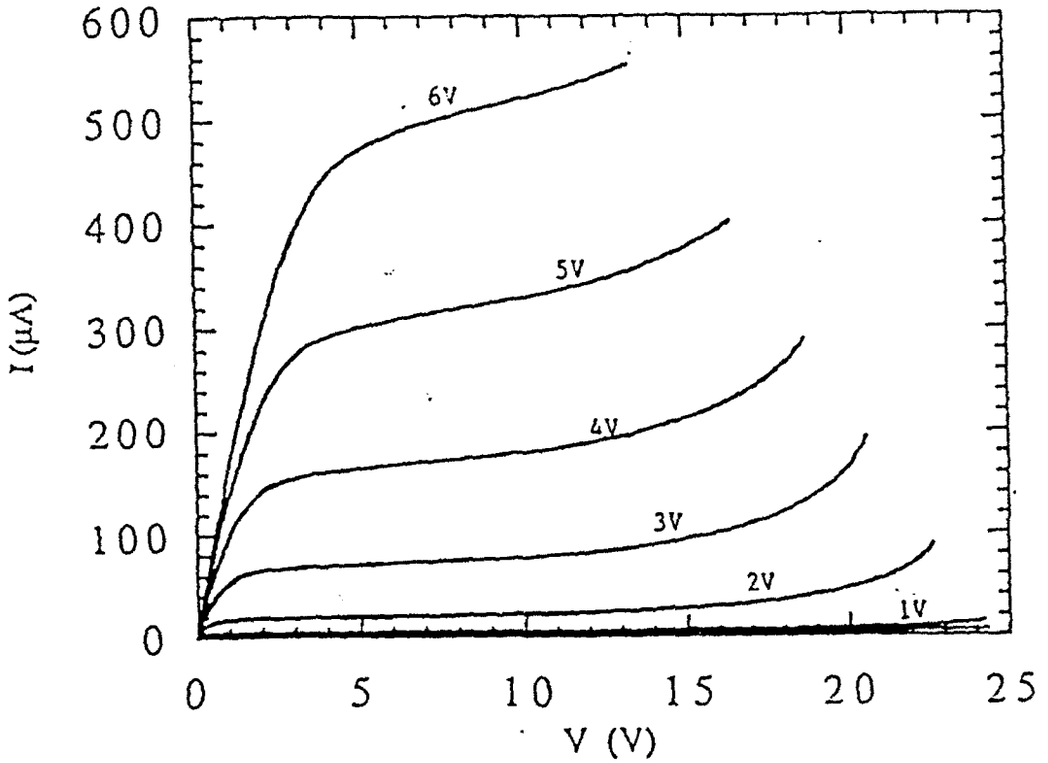


Figure 4. A typical I-V curve of NMOS transistor fabricated on bonded Si film.

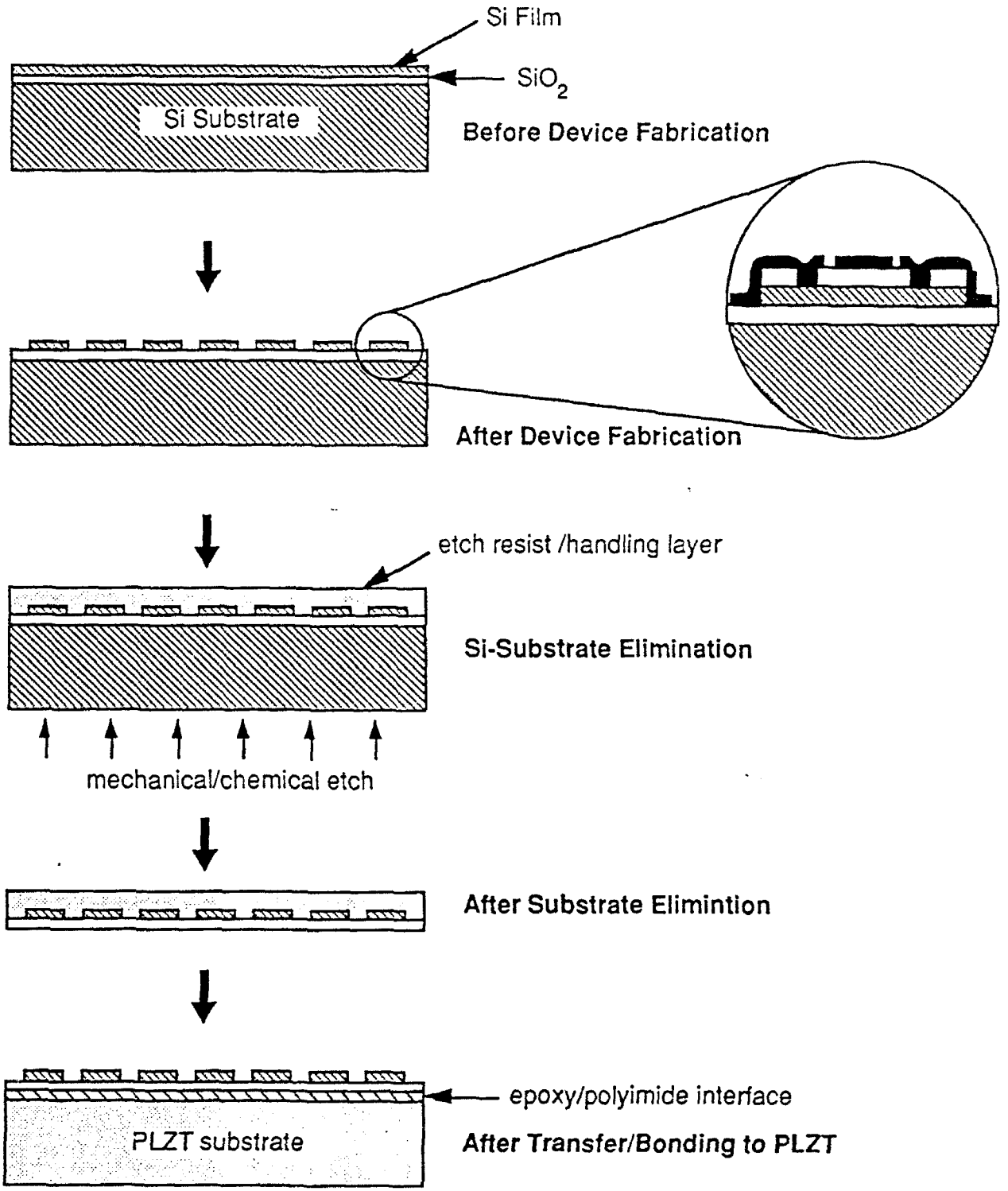
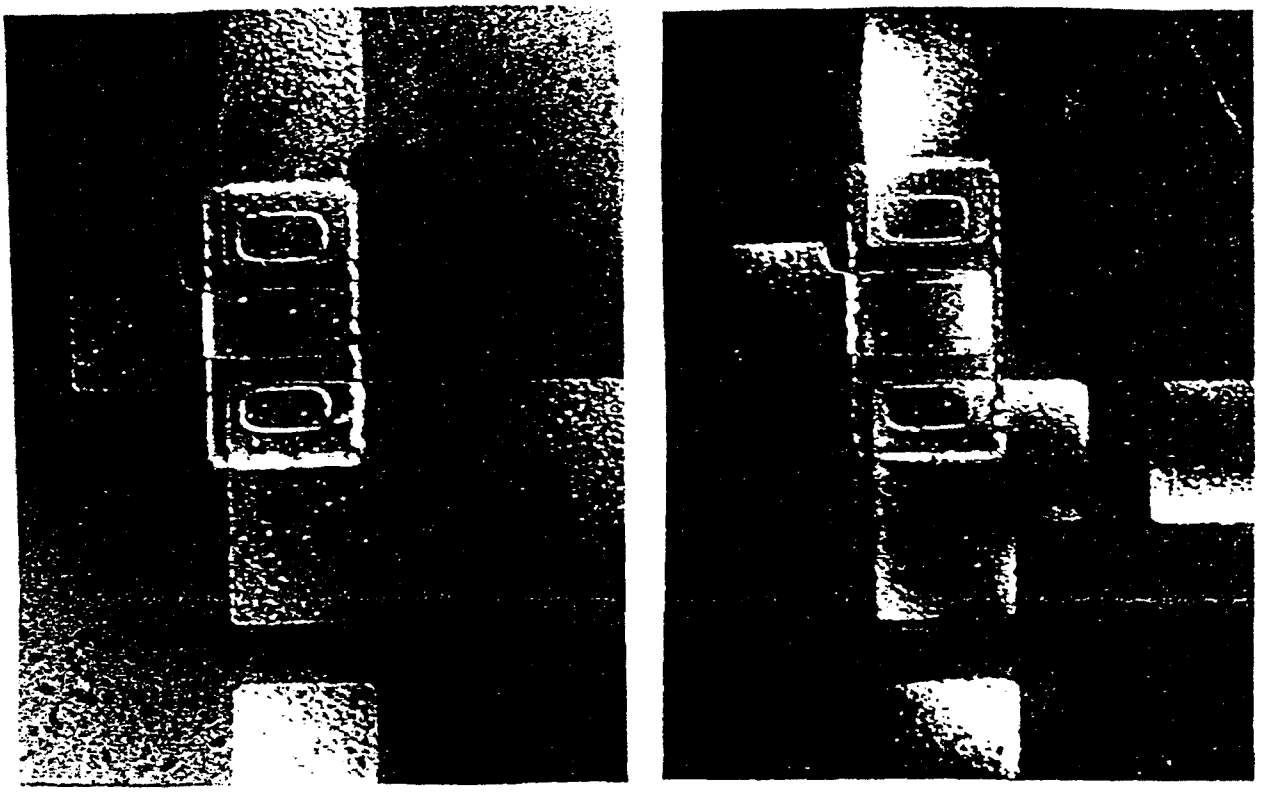


Figure 5. Schematic illustration of processing steps involved in thinning, transferring, and bonding pre-processed Si-device film onto PLZT substrate. In this approach, any standard Si-processing step can be applied.



(a) (b)

Figure 6. Photomicrograph of NMOS transistor (a) on host Si-substrate before and (b) on PLZT after the etch/transfer/bond.

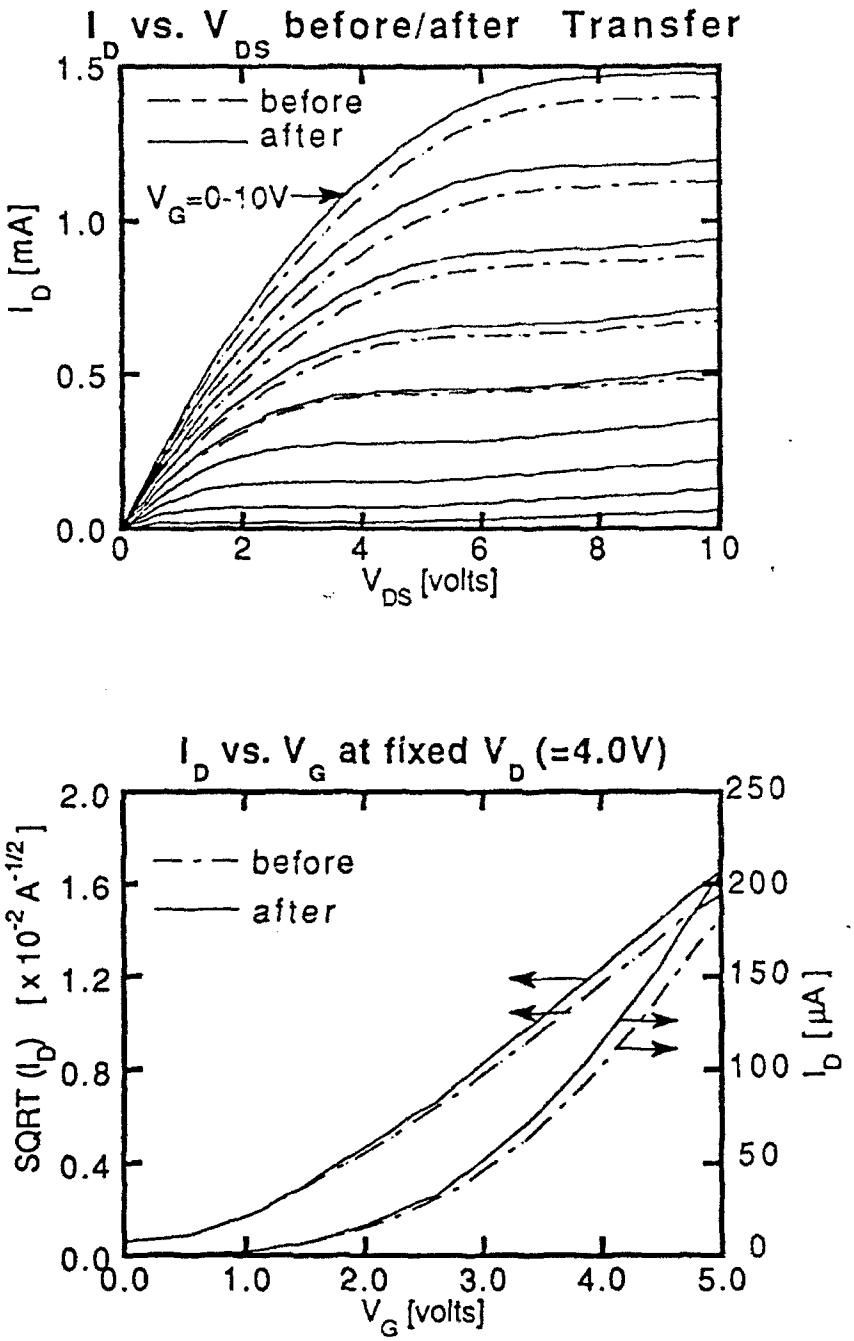
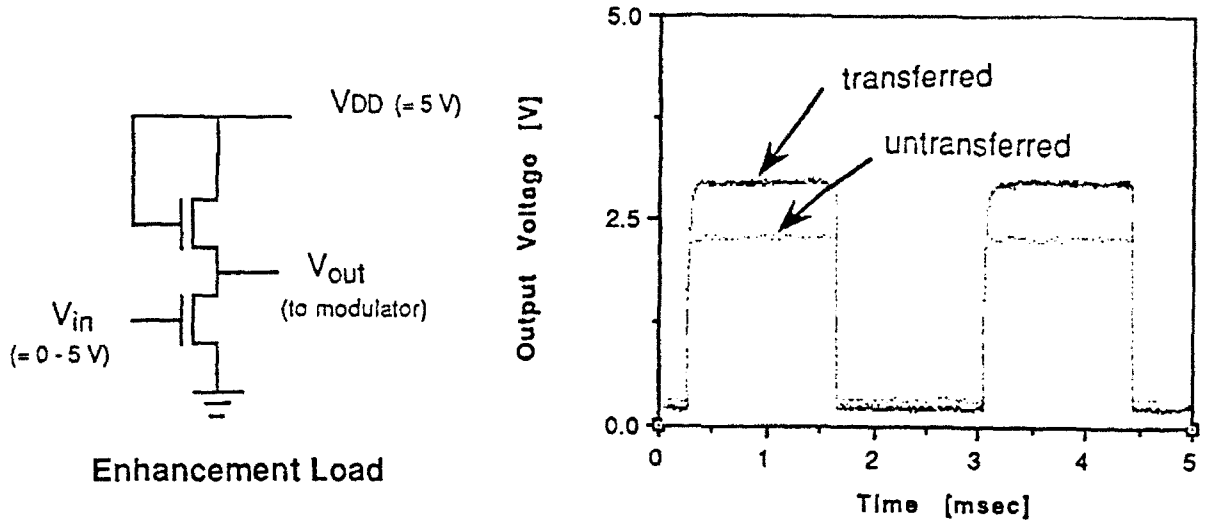
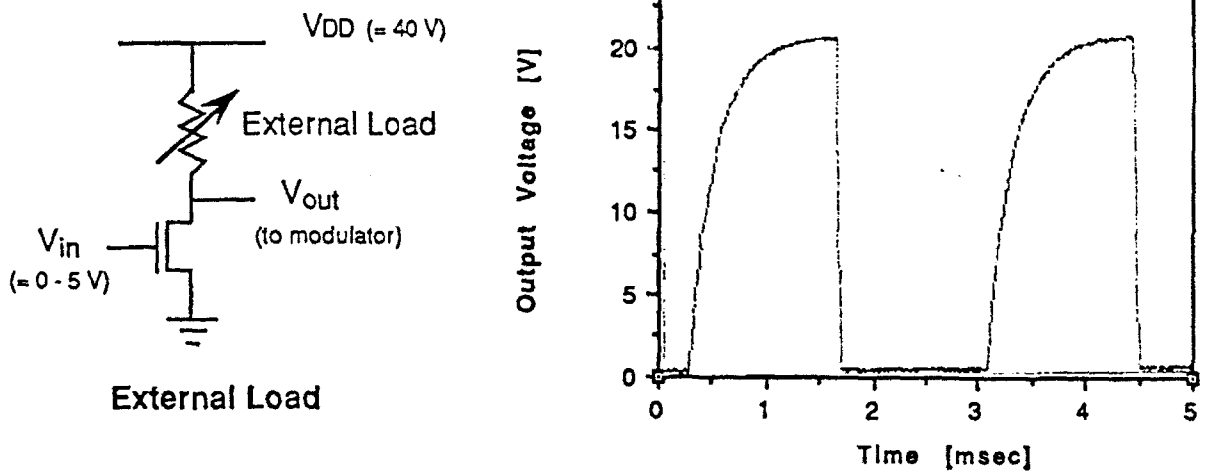


Figure 7. I-V curves of transistor of 10μm width and 20μm length gate size before and after the application of etch/transfer/ bond steps.



(a)



(b)

Figure 8. Inverter connection configurations and typical output traces for 0 - 5 V square input of devices processed with DB approach 2. (a) Actively-loaded (enhancement-load) inverter. The gate sizes of the corresponding transistors were L x W = 20 x 10 μm (for load transistor) and 20 x 40 μm (for inverting transistor). The output traces are that of a set of these transistors as-processed on SOI wafer (before) and after etch/transfer/bonding (after). (b) Externally-loaded inverter. The output trace is that of 20 x 40 μm gate transistor after etch/transfer/bonding.

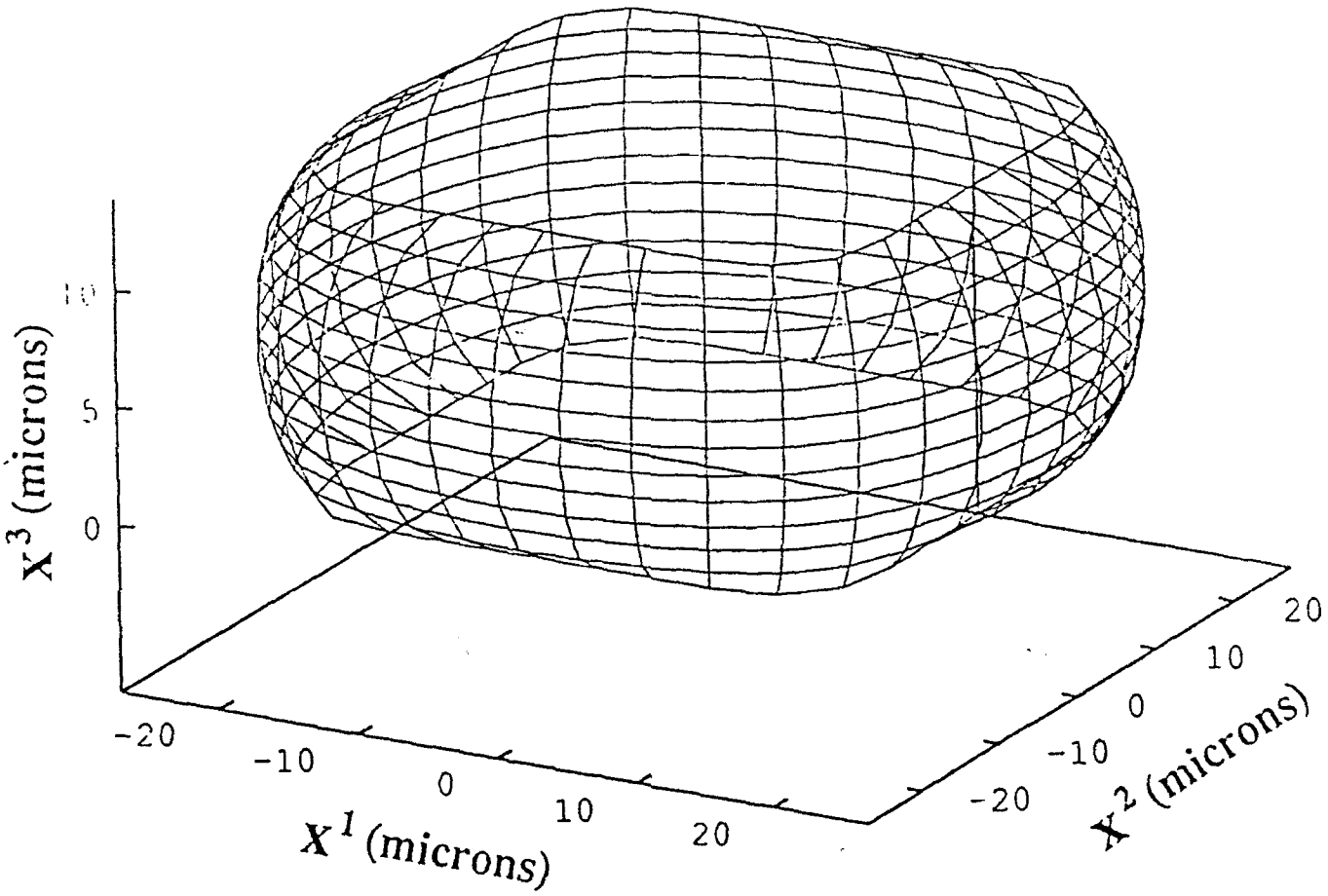


Figure 9. Solder joint profile for 40μm square pad and 20 μm solder deposition height.

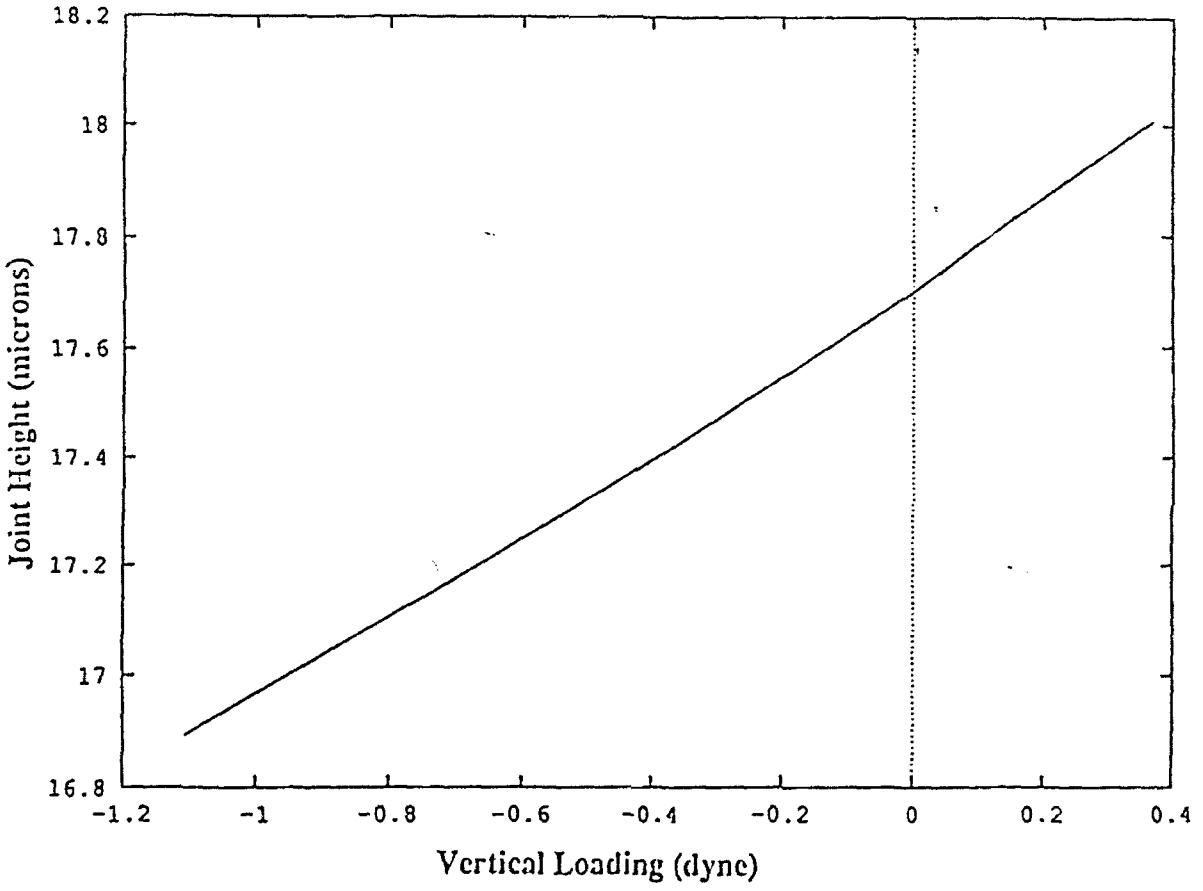


Figure 10. Solder joint height as a function of vertical loading.

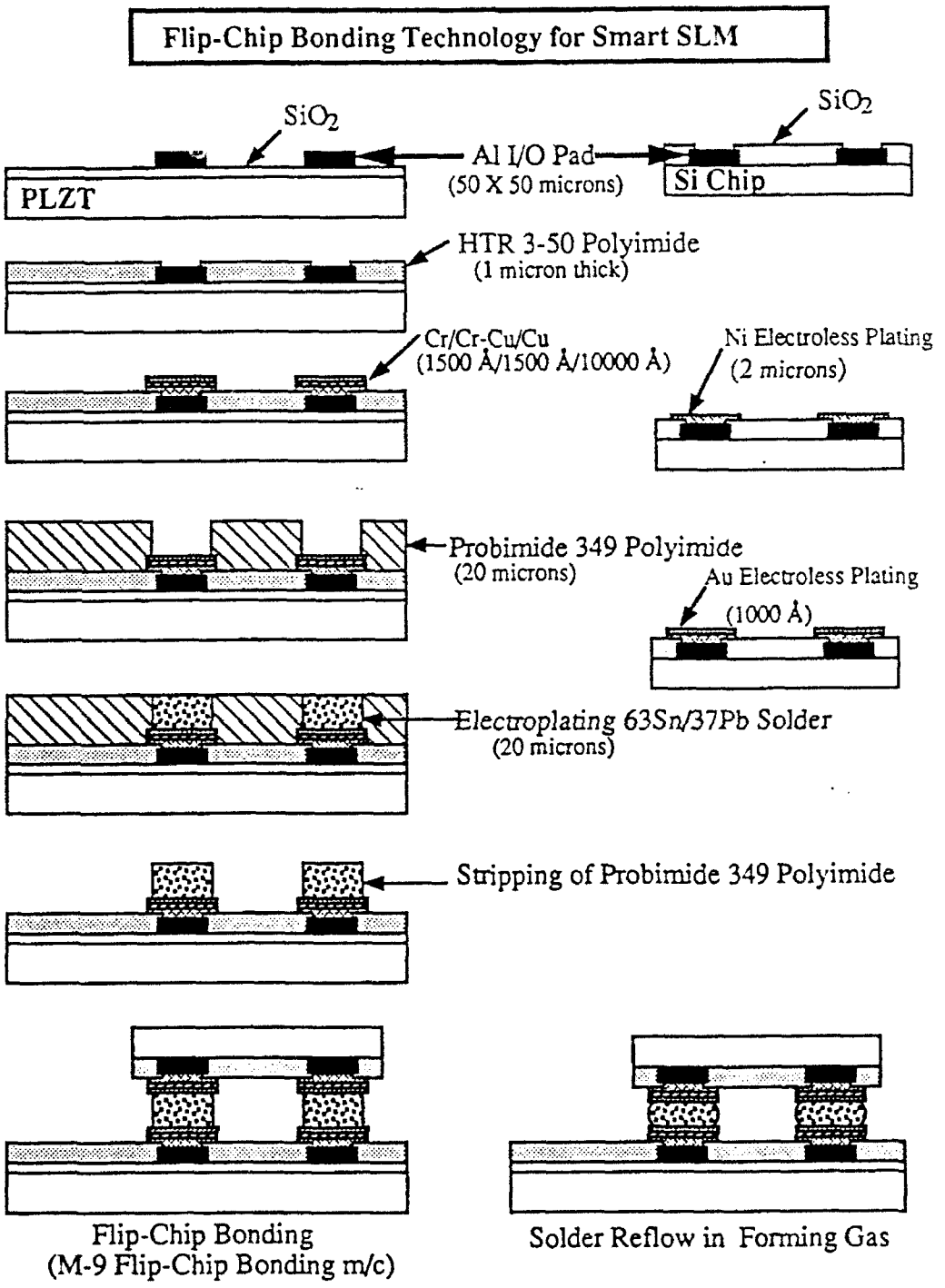


Figure 11. Process sequence for flip-chip bonding of S-SLM.

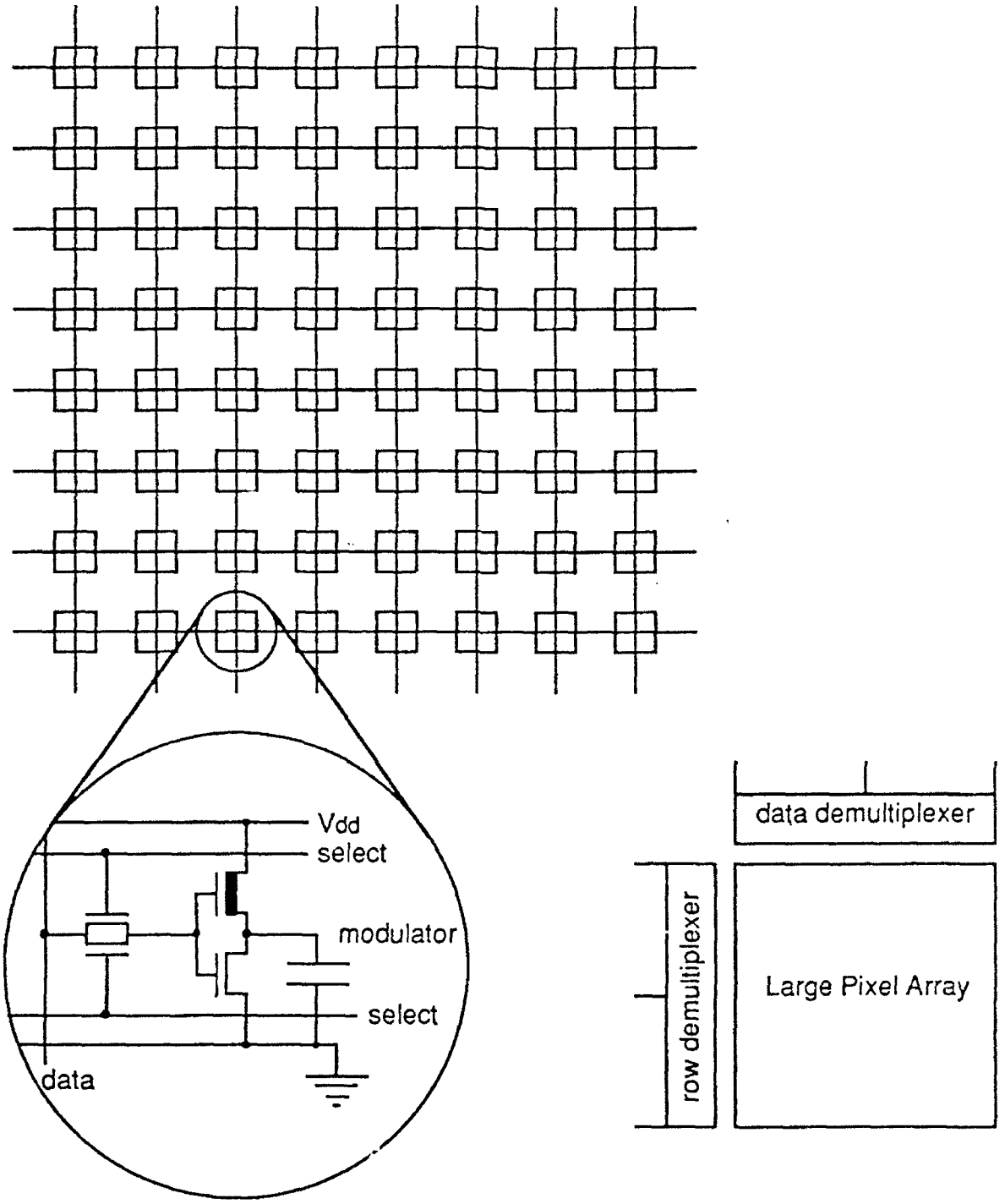


Figure 12. (a) Block diagram of 8x8 electrically-addressed SLM. (b) Demultiplexing for large arrays to keep the connection pin count low.

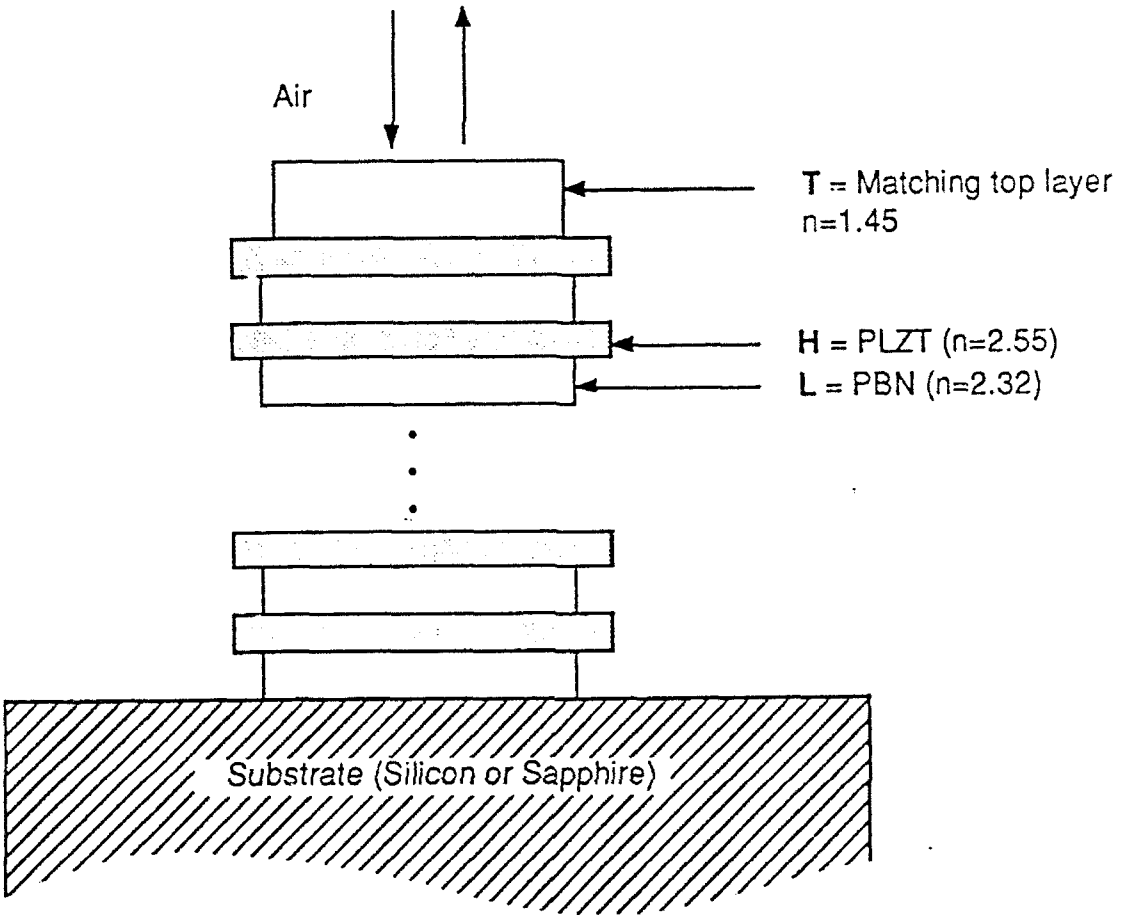


Figure 13. Schematic illustration of multilayer high reflector consisting of ferroelectric PLZT and PBN layers. Index matching top layer (T) suppresses the null value, inducing a substantial increase in contrast.

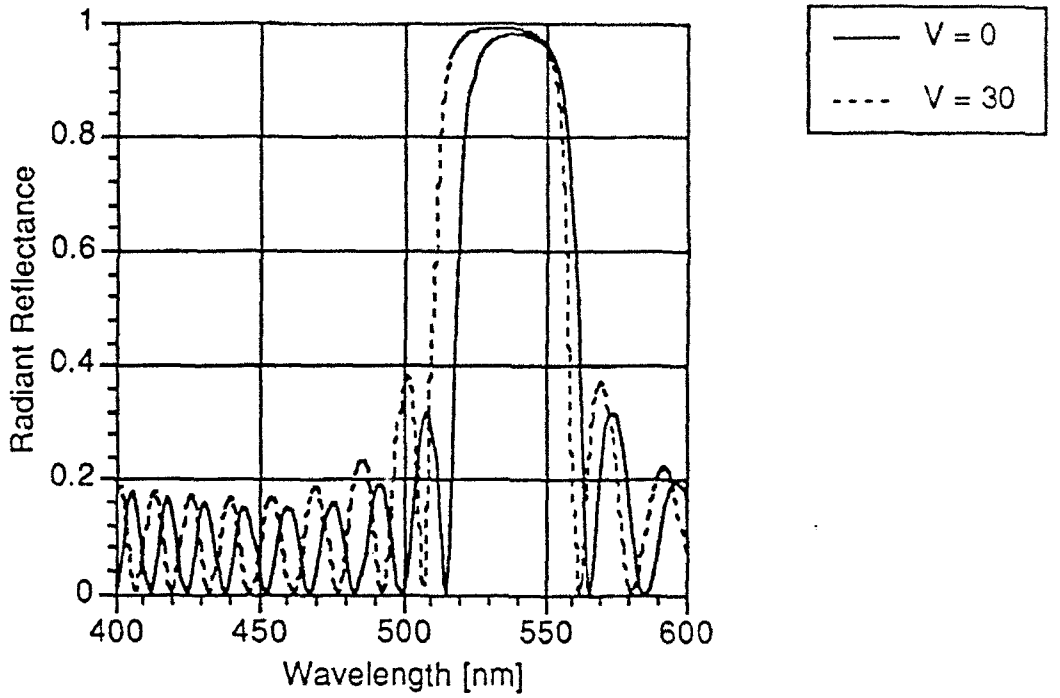


Figure 14. Wavelength spectrum of ferroelectric HR stack illustrated in Figure 13. The multilayer design is Air-T-$(HL)^{25}$-Silicon, where T, H and L are $\lambda/4$ optical thickness layers, with indices indicated in Figure 13, for design wavelength of λ = 538.8 nm; the design wavelength was selected so that the first minimum of the reflection band occurs on the operation wavelength λ_o = 514.5 nm. Total film thickness is ~3.0 μm. Electrode spacing of 10 μm is assumed. At the operation wavelength λ_o, R varies from 1.6×10^{-4} at V=0 to 0.8967 at V=30. Corresponding contrast is ~5600.

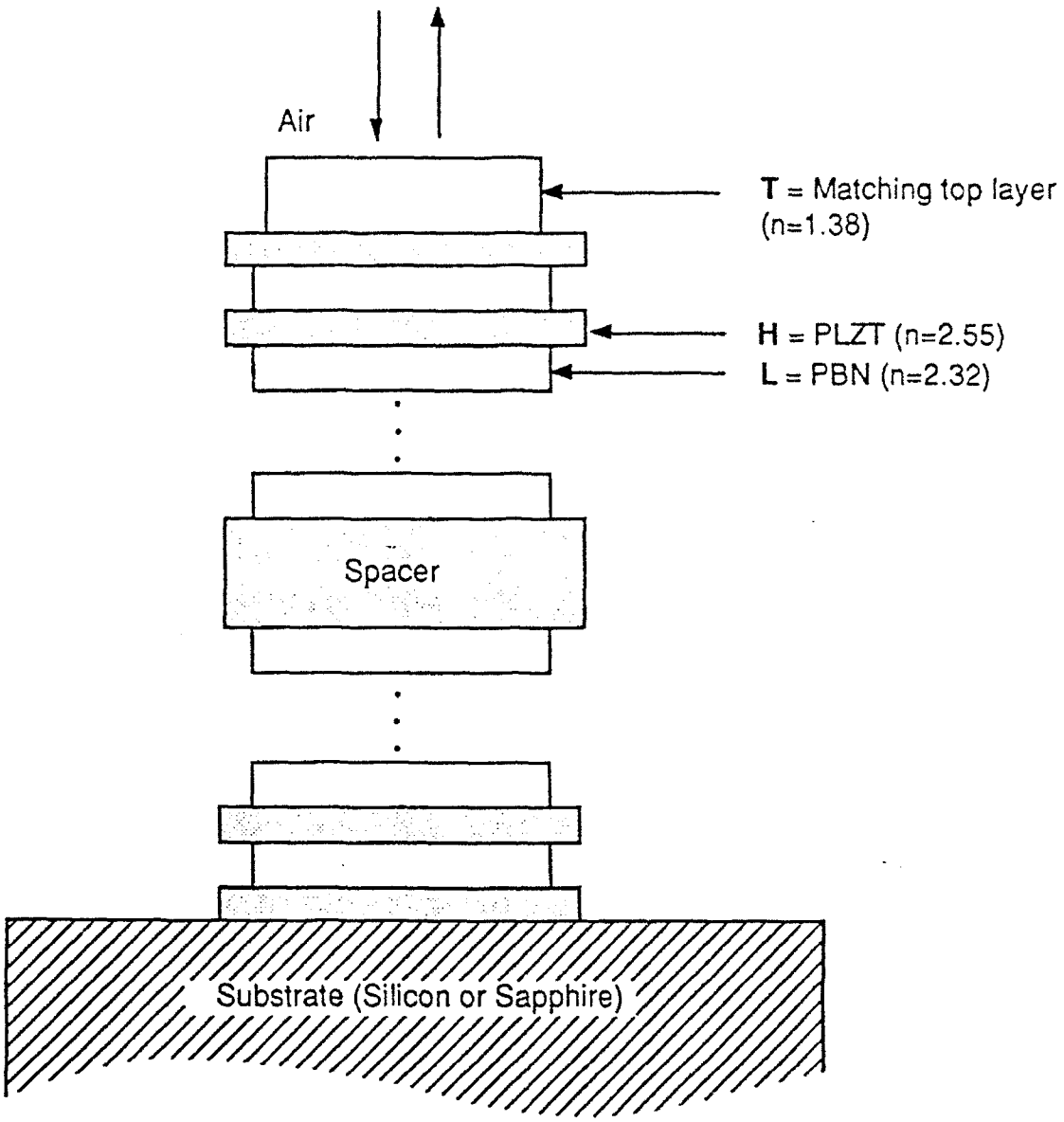


Figure 15. Schematic illustration of asymmetric Fabry-Perot modulator structure consisting of ferroelectric PLZT and PBN layers. Additional $\lambda/4$ thick layer on top of the active stack suppresses the null further.

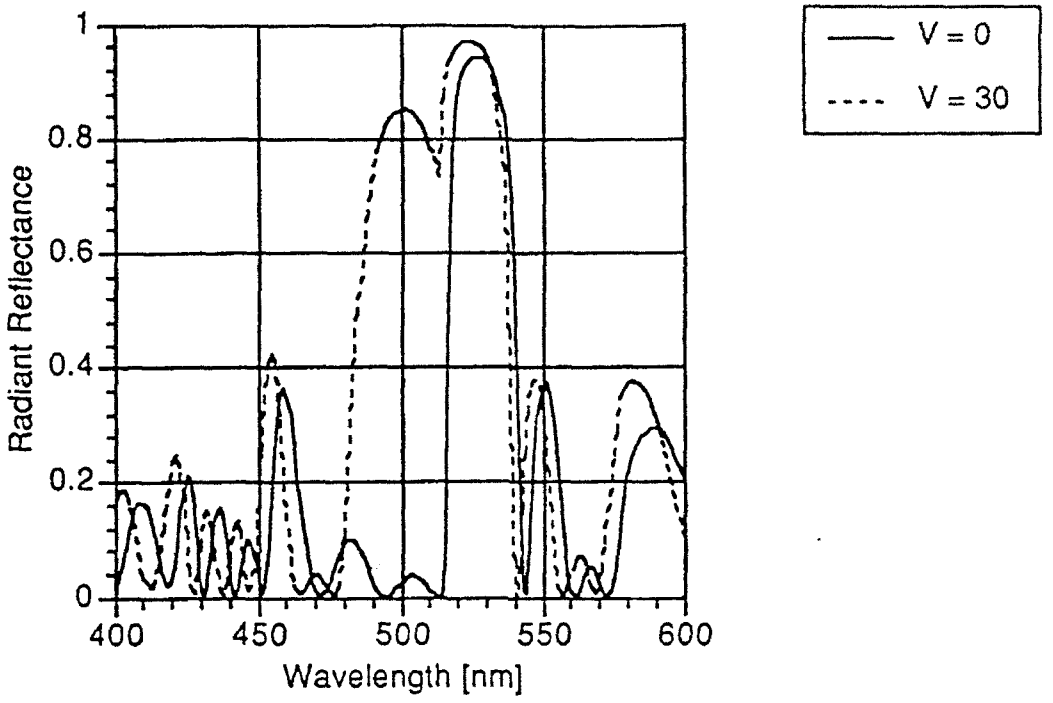


Figure 16. Wavelength spectrum of ferroelectric AFP modulator illustrated in Figure 15. The multilayer design is Air-T-$(HL)^{11}$-$(2H)^{9}$-$(HL)^{14}$-Silicon, where T, H and L are $\lambda/4$ optical thickness layers, with indices indicated in Figure 15, for λ=538.8 nm. Total film thickness is ~3.6 μm. Electrode spacing of 10 μm is assumed. For λ=514.5, R varies from 4.3×10^{-4} at V=0 to 0.8363 at V= 30. Corresponding contrast is ~1940.

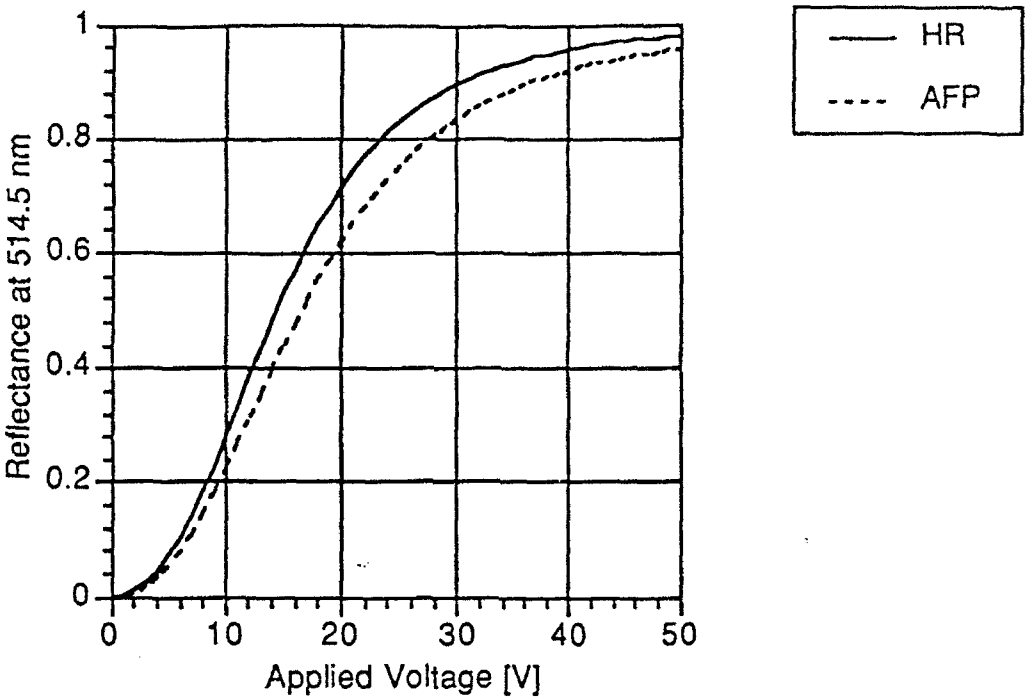


Figure 17. Radiant Reflectance *vs.* Applied Voltage curve at λ =514.5 for HR and AFP multilayers evaluated in Figures 14 and 16, respectively.